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CLAIM AMENDMENTS

1. (currently amended) A semiconductor device test apparatus comprising:

a test processor which applies a test signal to a semiconductor device under test and obtains information about a defective memory cell from a response signal; and

a repair analysis computing unit which performs repair analysis of the defective memory cell information to determine a way to repair the defective memory cell;

wherein the repair analysis computing unit comprises:

memory repair analysis means for performing repair analysis of the defective memory cell information in accordance with a memory repair analysis program based on regular defective memory cell repair conditions that are applicable to a regular type semiconductor device having a regular type memory structure and determining assignment of a spare line to the defective memory cell, said memory repair analysis program comprising operations constituting a process of repair analysis of the defective memory cell information; and

user function means for inserting ~~a user function based on user functions~~ of a user-specified user analysis program to user function insertion points between desired units of processing operations of the memory repair analysis program to make a change to data processed by the memory repair analysis program so that said memory repair analysis means performs repair analysis of the defective memory cell information based on specific defective memory cell repair conditions that are applicable to a specific type semiconductor device having a specific type memory structure other than the regular type memory structure.

2. (currently amended) The semiconductor device test apparatus according to claim 1, wherein the repair analysis computing unit comprises memory repair analysis public function means ~~which inserts for inserting~~ the user function ~~functions~~ to the user function insertion points ~~between desired units of processing of the memory repair analysis program through the intervention~~ of a memory repair analysis public function.

3. (currently amended) The semiconductor device test apparatus according to claim 2, wherein the memory repair analysis public function has a data check function portion which checks whether data set by the user function to determine whether the data is proper.

4. (currently amended) The semiconductor device test apparatus according to claim 1, wherein the repair analysis computing unit comprises:

a fail memory which stores the defective memory cell information ~~provided from the~~ test processor;

a memory repair analysis program storage section which stores the memory repair analysis program;

a user analysis program storage section which stores the user analysis program; and
an analysis control part which controls execution of the memory repair analysis program and execution of the user analysis program; and

the analysis control part and the memory repair analysis program storage section constitute the memory repair analysis means and the analysis control part ~~and~~ and
the user analysis program storage section constitute the user function means.

5. (currently amended) The semiconductor device test apparatus according to claim 4, wherein

the repair analysis computing unit has a repair condition file storage section which stores a plurality of repair condition files, each defining a repair condition for each type of semiconductor device;

the user analysis program storage section stores as the user analysis program a plurality of sets of user functions defined correspondingly to the plurality of repair condition files; and

the analysis control part selects a set of user functions on the basis of a repair condition file that matches the type of the semiconductor device under test and inserts the set of user functions ~~between units of processing of the memory repair analysis program to~~ the user function insertion points.

6. (currently amended) A semiconductor device test method comprising the steps of:

(a) performing a function test on a memory of a semiconductor device under test to obtain information about a defective memory cell;

(b) performing ~~memory~~ repair analysis of the defective memory cell information on a ~~processing unit by processing unit basis in accordance with a memory repair analysis program which comprises operations constituting a process of repair analysis of the defective memory cell information based on regular defective memory cell repair conditions that are applicable to a regular type semiconductor device having a regular type memory structure~~ to determine assignment of a spare line to the defective memory cell; and

(c) ~~inserting a user function based on a user-defined defective memory cell repair condition-functions of a user analysis program specified by user to user function insertion points between desired processing units-operations of the memory repair analysis program used at the step (b) to make a change to data processed by the memory repair analysis program so that repair analysis of the defective memory cell information is performed based on specific defective memory cell repair conditions that are applicable to a specific type semiconductor device having a specific type memory structure other than the regular type memory structure.~~

7. (currently amended) The semiconductor device test method according to claim 6, wherein the step (c) comprises ~~the step of inserting the user function between units of processing of the memory repair analysis program to the user function insertion points through the intervention of~~ a memory repair analysis public function.

8. (original) The semiconductor device test method according to claim 7, wherein the memory repair analysis public function comprises the step of executing a data check function which checks data set by the user function to determine whether the data is proper.

9. (currently amended) The semiconductor device test method according to claim 6, wherein

the memory repair analysis program comprises the steps of
performing line fail repair processing and
performing bit repair processing; and

~~step (c) comprises the step of~~

making a change to the result of the line fail repair processing through the user function after the step of performing the line fail repair processing and
~~the step of making a change to the result of the bit repair processing through~~
the user function after the step of performing the bit repair processing.

10. (currently amended) The semiconductor device test method according to claim 6,
wherein ~~the step (c) comprises the step of~~

selecting a set of user functions that corresponds to the type of the semiconductor device under test from among a plurality of sets of user functions provided correspondingly to a plurality of repair conditions predetermined for the types of semiconductor devices and
~~inserting the set of user functions between units of processing of the memory repair analysis program to the user function insertion points.~~